CLAIMS:

What is claimed is:

1. A data processing system, comprising:

an interrupt unit;

wherein the interrupt unit receives a signal for initiating an interrupt; and

wherein the interrupt unit counts the occurrence of interrupts by type.

2. The data processing system of claim 1, wherein a count value of an interrupt type is stored in an entry of an interrupt descriptor table.

3. The data processing system of claim 1, wherein a count value of an interrupt type is stored in an entry of an interrupt count table.

4. The data processing system of claim 3, wherein a count offset in an interrupt descriptor table corresponds to the interrupt type.

5. The data processing system of claim 4, wherein the count offset in the interrupt descriptor table is used to derive an offset address, corresponding to the count value of the interrupt type, in the interrupt count table.

6. The data processing system of claim 3, further comprising:

a register having a pointer to a memory address of the interrupt count table.

7. The data processing system of claim 1, further comprising hardware counters that count the occurrence of interrupts by type.

8. The data processing system of claim 1, wherein the types of interrupts include TLB (translation lookaside buffer) fault and VHPT (virtual hash page table) Instruction fault.

9. The data processing system of claim 1, wherein when a count is about to overflow, an overflow signal is sent.

10. A method for executing instructions on an information processing system, comprising the steps of:

receiving an interrupt signal at an interrupt unit, wherein the interrupt signal is for initiating an interrupt in a processor;

responsive to receiving the interrupt signal, incrementing a first counter based on a type of interrupt associated with the interrupt signal;

wherein the first counter is one of a plurality of counters; and

wherein the plurality of counters counts the occurrence of interrupts by type.

11. The method of claim 10, wherein a count value of the first counter is stored in an entry of an interrupt descriptor table.

12. The method of claim 10, wherein a count value of an interrupt type is stored in an entry of an interrupt count table.

13. The method of claim 12, wherein a count offset in an interrupt descriptor table corresponds to the interrupt type.

14. The method of claim 13, wherein the count offset in the interrupt descriptor table is used to derive an offset address, corresponding to the count value of the interrupt type, in the interrupt count table.

15. The method of claim 12, further comprising:

a register having a pointer to a memory address of the interrupt count table.

16. The method of claim 10, wherein the counters of the plurality are hardware counters.

17. The method of claim 10, wherein the types of interrupts include TLB (translation lookaside buffer) fault and VHPT (virtual hash page table) Instruction fault.

18. The method of claim 10, wherein when a count is about to overflow, an overflow signal is sent.

19. A computer program product in a computer readable medium, comprising:

first instructions for receiving an interrupt signal from an interrupt unit for initiating an interrupt in a processor;

second instructions for, responsive to receiving the interrupt signal, incrementing a first counter associated with the interrupt signal;

wherein the first counter is one of a plurality of counters; and

wherein the plurality of counters counts the occurrence of interrupts by type.

20. The computer program product of claim 19, wherein a count value of an interrupt type is stored in an entry of an interrupt descriptor table.

21. The computer program product of claim 19, wherein a count value of an interrupt type is stored in an entry of an interrupt count table.

22. The computer program product of claim 21, wherein a count offset in an interrupt descriptor table corresponds to an interrupt type.

23. The computer program product of claim 22, wherein the count offset in the interrupt descriptor table is

used to derive an offset address, corresponding to the count value of an interrupt type, in the interrupt count table.

24. The computer program product of claim 21, further comprising:

a register having a pointer to a memory address of the interrupt count table.

25. The computer program product of claim 19, wherein the counters of the plurality are hardware counters.

26. The computer program product of claim 19, wherein the types of interrupts include TLB (translation lookaside buffer) fault and VHPT (virtual hash page table) Instruction fault.

27. The computer program product of claim 19, wherein when a count is about to overflow, an overflow signal is sent.